IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A semiconductor device for use in a stacked multi-chip assembly, comprising:

a semiconductor die; and

a dielectric spacer layer, formed on at least a portion of a surface of ~~said~~the semiconductor die, and protruding therefrom substantially a predetermined distance that ~~said~~the semiconductor die and an adjacent semiconductor die of ~~said~~the stacked multi-chip assembly are to be spaced apart from one another, ~~said~~the spacer layer including voids communicating with a lateral periphery thereof.

2. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer comprises a plurality of laterally discrete spacers.

3. (Currently amended) The semiconductor device of claim 1, further comprising: at least one discrete conductive element protruding above a surface of ~~said~~the semiconductor die.

4. (Currently amended) The semiconductor device of claim 3, wherein ~~said~~the at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of ~~said~~the semiconductor die and ~~said~~the adjacent semiconductor die.

6. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of ~~said~~the semiconductor die and ~~said~~the adjacent semiconductor die.

7. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer covers only a portion of ~~said~~the surface.

8. (Currently amended) The semiconductor device of claim 7, wherein ~~said~~the dielectric spacer layer comprises a pattern.

9. (Currently amended) The semiconductor device of claim 7, wherein ~~said~~the dielectric spacer layer comprises randomly arranged features.

10. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer comprises a material that will adhere to a surface of ~~said~~the adjacent semiconductor die.

11. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer comprises a polymer.

12. (Currently amended) The semiconductor device of claim 11, wherein ~~said~~the polymer comprises a photoimageable polymer.

13. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer comprises at least one of a glass, a silicon dioxide, a silicon nitride, and a silicon oxynitride.

14. (Withdrawn and currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer is positioned on an active surface of ~~said~~the semiconductor die.

15. (Withdrawn and currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer is positioned on a back side of ~~said~~the semiconductor die.

16. (Withdrawn and currently amended) The semiconductor device of claim 1, further comprising:
another dielectric spacer layer covering at least a portion of an opposite surface of ~~said~~the semiconductor die.

17. (Currently amended) The semiconductor device of claim 1, further comprising:
adhesive material on an exposed surface of ~~said~~the dielectric spacer layer.

18. (Currently amended) The semiconductor device of claim 1, wherein ~~said~~the dielectric spacer layer comprises a plurality of at least partially superimposed, contiguous, adhered sublayers.

19. (Currently amended) A semiconductor device assembly, comprising:
a first semiconductor device;
a nonconfluent spacer layer comprising dielectric material and being positioned on a surface of ~~said~~the first semiconductor device; and
a second semiconductor device positioned over ~~said~~the first semiconductor device, a surface of ~~said~~the second semiconductor device being adhered to ~~said~~the nonconfluent spacer layer.

20. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of ~~said~~the nonconfluent spacer layer.

21. (Currently amended) The semiconductor device assembly of claim 20, wherein ~~said~~the at least one void facilitates lateral introduction of adhesive material between ~~said~~the first and second semiconductor devices.

22. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer has a substantially uniform thickness.

24. (Currently amended) The semiconductor device assembly of claim 19, further comprising:

at least one discrete conductive element protruding above a surface of at least one of ~~said~~the first and second semiconductor devices and located at least partially between ~~said~~the first and second semiconductor devices.

25. (Currently amended) The semiconductor device assembly of claim 24, wherein ~~said~~the nonconfluent spacer layer has a thickness that spaces ~~said~~the first and second semiconductor devices apart from one another a distance that exceeds a height ~~said~~the at least one discrete conductive element protrudes above ~~said~~the surface of at least one of ~~said~~the first and second semiconductor devices.

26. (Currently amended) The semiconductor device assembly of claim 24, wherein ~~said~~the nonconfluent spacer layer has a thickness that spaces ~~said~~the first and second semiconductor devices apart from one another a distance that is about the same as or less than a height ~~said~~the at least one discrete conductive element protrudes above ~~said~~the surface of at least one of ~~said~~the first and second semiconductor devices.

27. (Withdrawn and currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises dielectric material.

28. (Withdrawn and currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises a polymer.

29. (Withdrawn and currently amended) The semiconductor device assembly of claim 28, wherein ~~said~~the polymer adheres to surfaces of ~~said~~the first semiconductor device and ~~said~~the second semiconductor device.

30. (Withdrawn and currently amended) The semiconductor device assembly of claim 28, wherein ~~said~~the polymer comprises a photoimageable polymer.

31. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered sublayers.

32. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

33. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises a pattern.

34. (Withdrawn and currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer comprises randomly arranged features.

35. (Withdrawn and currently amended) The semiconductor device assembly of claim 19, further comprising:

an adhesive material securing ~~said~~the nonconfluent spacer layer to at least one of ~~said~~the surface of ~~said~~the first semiconductor device and ~~said~~the surface of ~~said~~the second semiconductor device.

36. (Withdrawn and currently amended) The semiconductor device assembly of claim 35, wherein ~~said~~the adhesive material is located within voids in ~~said~~the nonconfluent spacer layer.

37. (Currently amended) The semiconductor device assembly of claim 19, further comprising:

a substrate upon which one of ~~said~~the first semiconductor device and ~~said~~the second semiconductor device is positioned.

38. (Currently amended) The semiconductor device assembly of claim 37, wherein at least one bond pad of at least one of ~~said~~the first semiconductor device and ~~said~~the second semiconductor device is in communication with a corresponding contact area of ~~said~~the substrate.

39. (Currently amended) The semiconductor device assembly of claim 37, wherein ~~said~~the substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

40. (Currently amended) The semiconductor device assembly of claim 19, wherein ~~said~~the nonconfluent spacer layer is positioned between an active surface of ~~said~~the first semiconductor device and a back side of ~~said~~the second semiconductor device.

41. (Withdrawn and currently amended) The semiconductor device assembly of claim 19, further comprising:
at least one additional semiconductor device.

42. (Currently amended) The semiconductor device assembly of claim 19, further comprising:
a plurality of nonconfluent spacer layers between ~~said~~the first and second semiconductor devices, additive thicknesses of ~~said~~the plurality of nonconfluent spacer layers defining a distance ~~said~~the first and second semiconductor devices are spaced apart from one another.

43. (Currently amended) The semiconductor device assembly of claim 42, wherein a first nonconfluent spacer layer of ~~said~~the plurality of nonconfluent spacer layers is secured to a surface of ~~said~~the first semiconductor device and a second nonconfluent spacer layer of ~~said~~the plurality of nonconfluent spacer layers is secured to an opposed surface of ~~said~~the second semiconductor device.

44. (Currently amended) The semiconductor device assembly of claim 42, wherein at least some solid regions of each of ~~said~~the plurality of nonconfluent spacer layers are at least partially superimposed relative to one another.

45. (Withdrawn and currently amended) A multi-chip module, comprising:
a substrate;
a first semiconductor device positioned on ~~said~~the substrate;
a nonconfluent layer comprising dielectric material over ~~said~~the first semiconductor device;
a second semiconductor device positioned over ~~said~~the nonconfluent layer; and
an encapsulant covering at least portions of ~~said~~the first semiconductor device, ~~said~~the nonconfluent layer, ~~said~~the second semiconductor device, and portions of ~~said~~the substrate located adjacent ~~said~~the first semiconductor device.

46. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

47. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein at least one bond pad of at least one of ~~said~~the first semiconductor device and ~~said~~the second semiconductor device is in electrical communication with a corresponding contact area of ~~said~~the substrate.

48. (Withdrawn and currently amended) The multi-chip module of claim 47, wherein ~~said~~the electrical communication is established by at least one discrete conductive element extending at least partially between ~~said~~the first and second semiconductor devices and protruding above a surface of at least one of ~~said~~the first semiconductor device and ~~said~~the second semiconductor device.

49. (Withdrawn and currently amended) The multi-chip module of claim 48, wherein ~~said~~the nonconfluent layer has a thickness that exceeds a distance ~~said~~the at least one discrete conductive element protrudes above ~~said~~the surface.

50. (Withdrawn and currently amended) The multi-chip module of claim 48, wherein a thickness of ~~said~~the nonconfluent layer is about the same as or less than a distance ~~said~~the at least one discrete conductive element protrudes above ~~said~~the surface.

51. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

52. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent layer comprises a pattern.

53. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent layer comprises randomly arranged features.

54. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent layer has a substantially consistent height.

55. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent layer comprises a dielectric material.

56. (Withdrawn and currently amended) The multi-chip module of claim 55, wherein ~~said~~the dielectric material comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

57. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent layer comprises a polymer.

58. (Withdrawn and currently amended) The multi-chip module of claim 57, wherein ~~said~~the polymer is capable of adhering to a surface of at least one of ~~said~~the first semiconductor device and ~~said~~the second semiconductor device.

59. (Withdrawn and currently amended) The multi-chip module of claim 57, wherein ~~said~~the polymer comprises a photoimageable polymer.

60. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the nonconfluent layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered layers.

61. (Withdrawn and currently amended) The multi-chip module of claim 45, further comprising:

an adhesive material securing ~~said~~the first and second semiconductor devices to one another.

62. (Withdrawn and currently amended) The multi-chip module of claim 61, wherein ~~said~~the adhesive material is located within voids of ~~said~~the nonconfluent layer.

63. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the encapsulant comprises a glob-top type encapsulant.

64. (Withdrawn and currently amended) The multi-chip module of claim 45, wherein ~~said~~the encapsulant comprises a molded encapsulant.

65. (Withdrawn and currently amended) The multi-chip module of claim 45, further comprising:
a plurality of nonconfluent layers between ~~said~~the first and second semiconductor devices, additive thicknesses of ~~said~~the plurality of nonconfluent layers defining a distance ~~said~~the first and second semiconductor devices are spaced apart from one another.

66. (Withdrawn and currently amended) The multi-chip module of claim 65, wherein a first nonconfluent layer of ~~said~~the plurality of nonconfluent layers is secured to a surface of ~~said~~the first semiconductor device and a second nonconfluent layer of ~~said~~the plurality of nonconfluent layers is secured to an opposed surface of ~~said~~the second semiconductor device.

67. (Withdrawn and currently amended) The multi-chip module of claim 65, wherein at least some solid regions of each of ~~said~~the plurality of nonconfluent layers are at least partially superimposed relative to one another.

68-102. (cancelled)

REMARKS

The Final Office Action dated August 20, 2003, has been received and reviewed.

Claims 1-67 remain pending in the above-referenced application. Of these, claims 14-16, 27-30, 34-36, 41, and 45-67 have been withdrawn from consideration as being drawn to non-elected inventions. Claims 1-13, 17-26, 31-33, 37-40, and 42-44, which have been considered, stand rejected. Claims 68 through 102 have been canceled without prejudice or disclaimer.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-11, 13, 17-26, 31-33, 37-40, and 42-44 stand rejected under 35 U.S.C. § 102(b) for purportedly reciting subject matter which is anticipated by the described in U.S. Patent 6,472,758 to Glenn et al. (hereinafter "Glenn").

Case law and the M.P.E.P. both hold that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Furthermore, the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Additionally, the elements must be arranged as required by the claim, but identity of the terminology is not required. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990).

Glenn describes, among other things, an adhesive 40 for use as a spacer layer 42 between stacked semiconductor devices. Col. 7, lines 5-11. The adhesive 40 may be filled with microspheres 48. *Id.* The disclosure of Glenn appears to be limited to use of solid microspheres 48 in the spacer layer 42. *See* col. 7, lines 26-43. The microspheres 48, which are useful for "precisely controlling the final bond line thickness of the adhesive layer **42** distributed between the opposing surfaces of . . . two dies **14** and **16**," (col. 7, lines 1-5 and 12-16) appear to be completely laterally surrounded by the adhesive material 40.

Independent claim 1 is drawn to a semiconductor device for use in a stacked multi-chip assembly. The semiconductor device includes a semiconductor die and a dielectric spacer layer on at least a portion of a surface of the semiconductor die. The dielectric spacer layer includes "voids communicating with a lateral periphery thereof."

It is respectfully submitted that Glenn lacks any express or inherent description of voids in layer 42, let alone voids that communicate with a lateral periphery of spacer layer 42. As for the assertion that the spaces between adjacent microspheres 48 comprise voids, Glenn does not expressly or inherently describe that the microspheres 48 may, by themselves, comprise a spacer layer 42. To do so, the microspheres would have to be held in position relative to at least one of the stacked semiconductor dies 14, 16. Nonetheless, Glenn lacks any express or inherent description that the microspheres 48 may be put into place independently of the adhesive material 40.

As such, it is respectfully submitted that Glenn does not anticipate each and every element of independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(e). Therefore, under 35 U.S.C. § 102(e), independent claim 1 is allowable over Glenn.

Claims 2-11, 13, 17, and 18 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 6 is also allowable because Glenn does not expressly or inherently describe a dielectric spacer layer that protrudes from a surface of a semiconductor die a distance which is "about the same as or less than a distance a discrete conductive element protrudes above [the] surface" of at least one of the semiconductor die and another, adjacent semiconductor die.

Claim 16 is further allowable since Glenn neither expressly nor inherently describes a semiconductor device that includes a semiconductor die with spacer layers on both surfaces thereof.

Claim 18 is additionally allowable since Glenn does not expressly or inherently describe a semiconductor device with a dielectric spacer layer that includes "a plurality at least partially superimposed, contiguous, adhered sublayers."

Independent claim 19 recites a semiconductor device assembly that includes first and second semiconductor devices, as well as a nonconfluent spacer layer therebetween.

Again, it is respectfully submitted that Glenn neither expressly nor inherently describes that the spacer layer 42 disclosed therein is nonconfluent. While the spacer layer 42 of Glenn may include microspheres 48, Glenn does not expressly or inherently describe that the microspheres 48 may be hollow or otherwise configured in such a way as to render the spacer layer 42 nonconfluent. Rather, based on the description that has been provided by Glenn, the microspheres 48 would be solid structures that form part of a solid, confluent spacer layer 42.

For these reasons, it is respectfully submitted that independent claim 19 recites subject matter which is not anticipated under 35 U.S.C. § 102(e). Thus, under 35 U.S.C. § 102(e), independent claim 19 is allowable over the subject matter described in Glenn.

Each of claims 20-26, 31-33, 37-40, and 42-44 is allowable, among other reasons, for depending either directly or indirectly from claim 19, which is allowable.

Claim 20 is further allowable because Glenn lacks any express or inherent description of a nonconfluent spacer layer that includes "at least one void therein that communications with a lateral periphery of [the] nonconfluent spacer layer." Rather, the description of Glenn is limited to mixing microspheres 48 into a quantity of adhesive material 40 prior to placing the microspheres 48 onto a surface of a semiconductor die. Thus, there are no voids in the resulting layer 42.

Claim 21, which depends from claim 20, is also allowable since Glenn does not expressly or inherently describe a spacer layer which includes at least one void that "facilitates lateral introduction of adhesive material between . . . first and second semiconductor devices." Instead, the description of Glenn is limited to mixing microspheres 48 into a quantity of adhesive material 40 prior to placing the microspheres 48 onto a surface of a semiconductor die. Accordingly, there are no voids in the resulting layer 42 into which adhesive material may be laterally introduced.

Claim 26 is also allowable because Glenn does not expressly or inherently describe a dielectric spacer layer that protrudes from a surface of a semiconductor die a distance which is "about the same as or less than a height the at least one discrete conductive element protrudes

above the surface" of at least one of the semiconductor die and another, adjacent semiconductor die.

Claim 31 is additionally allowable since Glenn does not expressly or inherently describe a semiconductor device with a dielectric spacer layer that includes "a plurality at least partially superimposed, contiguous, mutually adhered sublayers."

Claim 41 is further allowable since Glenn lacks any express or inherent description of a semiconductor device assembly that includes more than two semiconductor devices.

Claim 42 is additionally allowable because Glenn neither expressly nor inherently describes a semiconductor device assembly that includes "a plurality of nonconfluent spacer layers between . . . first and second semiconductor devices."

Claim 43 depends from claim 42 and is also allowable since Glenn includes no express or inherent description of different nonconfluent spacer layers that are secured to opposed surfaces of different, first and second semiconductor devices.

Claim 44 also depends from claim 42, and is additionally allowable since Glenn neither expressly nor inherently describes a semiconductor device assembly with a plurality of at least partially superimposed spacer layers between two semiconductor devices.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1-11, 13, 17-26, 31-33, 37-40, and 42-44 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 12, 13, and 32 stand rejected under 35 U.S.C. § 103(a).

The standard for a 35 U.S.C. § 103(a) rejection is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

> limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Glenn in View of Smith

Claim 12 stands rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Glenn, in view of teachings from U.S. Patent 6,049,370 to Smith, Jr. et al. (hereinafter "Smith").

Claim 12 is allowable, among other reasons, for depending from claim 1, which is allowable.

Glenn et al. in View of Mueller et al.

Claims 13 and 32 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over teachings from Glenn, in view of teachings of U.S. Patent 6,316,786 to Mueller et al. (hereinafter "Mueller").

Claim 13 is allowable, among other reasons, for depending from claim 1, which is allowable.

Claim 32 is allowable, among other reasons, for depending from claim 19, which is allowable.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 12, 13, and 32 be withdrawn.

ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claims 1 and 19 remain generic to all of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41, and 45-67, which have been withdrawn from consideration, should also be allowed.

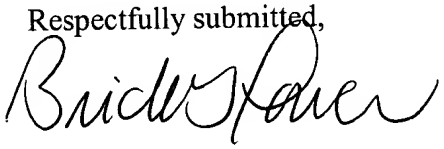
ENTRY OF AMENDMENTS

It is respectfully submitted that the claim amendments that have been proposed herein should be entered since they do not introduce new matter into the above-referenced application and they will not necessitate an additional search. In all instances, the amendatory language involves replacement of the term "said" with the word "the." No substantive amendments are proposed. In the event that the proposed claim amendments are not entered, entry thereof upon filing of a Notice of Allowance in the above-referenced application is respectfully requested.

CONCLUSION

It is respectfully submitted that each of claims 1-67 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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